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ScienceDirect
International Journal of Heat and Mass Transfer 50 (2007) 4767–4779
International Journal of HEAT and MASS TRANSFER
www.elsevier.com/locate/ijhmt

Experimental investigation of microchannel coolers for the high heat flux thermal management of GaN-on-SiC semiconductor devices

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Received 8 February 2006; received in revised form 28 February 2007
Available online 30 April 2007

Abstract

Experiments on removing high heat fluxes from GaN-on-SiC semiconductor dies using microchannel coolers are described. The dies contain an AlGaN/GaN heterostructure operated as a direct current resistor, providing a localized heat source. The active dimensions of the heat source are sized to represent the spatially-averaged heat flux that would appear in microwave power amplifiers. A wide variety of microchannel materials and configurations are investigated, allowing a comparison of performance and the resulting GaN temperatures. Silicon and AlN microchannel coolers exhibit good performance at lower power densities (1000–1200 W/cm^2 over 3×5 mm^2 to 2×5 mm^2 active areas). Polycrystalline chemical vapor deposited (CVD) SiC microchannel coolers are found to be extremely promising for higher power densities (3000–4000 W/cm^2 over 1.2×5 mm^2 active areas with 120 °C GaN temperature). A hybrid microchannel cooler consisting of low-cost CVD diamond on polycrystalline CVD SiC exhibits moderately better performance (20–30%) than polycrystalline CVD SiC alone.

Keywords: Microchannel cooler; Single phase flow; Electronic packaging; Diamond

1. Introduction

Wide bandgap semiconductor technology, based around SiC and GaN, has excellent potential for high-power applications, including microwave devices and power switching electronics [1]. This is due to the combination of high electron sheet charge density and saturation velocity, good electron mobility, and in particular, the very high breakdown electric field strength of wide bandgap materials compared to Si, GaAs, and InP semiconductors [1], as listed in Table 1. A device of particular importance for microwave applications is the AlGaN/GaN high electron mobility transistor (HEMT) [2], consisting of a horizontal electrically conducting channel with source, gate, and drain metallizations, as shown in the layout of Fig. 1a. The gate is very short in the x-direction, typically with L_G of 0.5 μm or less. For high power operation, such HEMTs are grown by chemical vapor deposition (CVD) processes on high thermal conductivity, single crystal SiC substrates, typically semi-insulating 4H–SiC or 6H–SiC. In laboratory settings, such HEMTs have produced 5–10 W of microwave power per mm of gate width w (in the y-axis direction), with isolated experiments near 30 W/mm [2,3]. These values are factors of 4–25 above any competing technologies. The dissipated power densities directly under the miniscule gates in the GaN-based HEMTs are incredible, of order 1–2 MW/cm^2, but in test devices with a very modest total gate width ($\leqslant$0.3 mm), the heat easily spreads in a 3D fashion into the substrate and the thermal management problem is not particularly vexing.

However, when one wants to generate much larger total powers by increasing the total gate width, for various technical reasons, it is necessary to use a multi-fingered HEMT layout as shown in Fig. 1b. Briefly, the layout is necessary to avoid signal transmission losses due to distributed gate

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doi:10.1016/j.ijheatmasstransfer.2007.03.013

Nomenclature

d	microchannel width (m)
D	microchannel hydraulic diameter (m)
f	friction factor
F_H	heat flux (W/cm^2)
h	heat transfer coefficient (W cm^{-2} K^{-1})
h_{wall}	microchannel wall heat transfer coefficient (W cm^{-2} K^{-1})
L_{active}	length of active region on the die (m)
L_G	transistor gate length (m)
L_p	gate-to-gate pitch spacing (m)
Nu	Nusselt number
Pr	Prandtl number
$P_{W(waste)}$	waste heat dissipated per unit gate width (W/mm)
Re	Reynolds number for microchannel
t	microchannel height (m)
T_B	bulk fluid temperature (°C)
w	transistor gate width (m)

Greek symbols

κ	thermal conductivity of the microchannel cooler material (W m^{-1} K^{-1})
κ_f	thermal conductivity of the fluid (W m^{-1} K^{-1})

Table 1
Properties of semiconductor materials and heterostructures

Material property	Material (heterostructure)				
	Si	GaAs (AlGaAs/InGaAs)	InP (InAlAs/InGaAs)	4 H–SiC	GaN(AlGaN/GaN)
Bandgap (eV)	1.10	1.42	1.35	3.26	3.49
Electron mobility (m^2 V^{-1} s^{-1})	0.15	0.85 (1.0)	0.54 (1.0)	0.070	0.090 (>0.2)
Saturated electron velocity (m/s)	1.0×10^5	1.0×10^5	1.0×10^5	2.0×10^5	1.5×10^5
Electron sheet charge density (m^{-2})	–	4×10^{16}	4×10^{16}	–	$1–2 \times 10^{17}$
Breakdown electric field (MV m^{-1})	30	40	50	200	330
Thermal conductivity (W m^{-1} K^{-1})	150	50	70	450	130–170

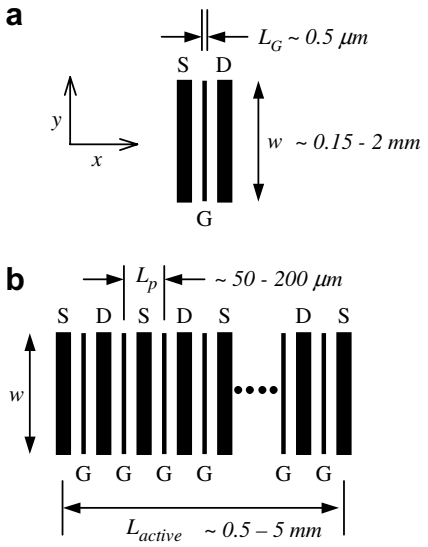

Fig. 1. Top view of transistor layouts, showing (a) single and (b) multi-fingered configurations. Source (S), gate (G), and drain (D) metallizations are indicated. The electrically conducting channel and the underlying substrate die are beneath the metallizations in the plane of the paper.

resistance and gate capacitance that would occur along a single, extremely wide gate, as well as to minimize electromagnetic time delay (phasing) problems. The layout of Fig. 1b also helps conserve expensive substrate area. When one contemplates creating microwave devices and monolithic microwave integrated circuits (MMICs) with total power dissipations of 100 or even 300 W, the dimensions of this "active area" $w \times L_{active}$ enclosing the fingers can become substantial, from several mm^2 to 10 mm^2, depending on the operating frequency. The spatially-averaged power density within the active area [4,5] is the W/mm waste heat dissipation per unit gate width $P_{W(waste)}$, divided by the gate-to-gate pitch spacing L_p in Fig. 1b. So for 5 W/mm $P_{W(waste)}$ and a typical 50 μm pitch, the spatially-averaged power density is 10 kW/cm^2; even for a much more generous 200 μm pitch it is 2.5 kW/cm^2. For a 200 W dissipation device, the relevant areas are 2 and 8 mm^2, for the 50 and 200 μm pitch, respectively.

Removing these levels of total power and heat flux is a challenging problem if a reasonable HEMT gate temperature (150–175 °C) is to be maintained [4,5]. Although still localized, the peak heat fluxes appearing on the rear of a typical 100–380 μm thick substrate die are expected to be several kW/cm^2, so techniques of removing high heat fluxes are of paramount importance. An example of the simulated temperature profiles in the x-direction for a multi-fingered HEMT structure (at 5 W/mm $P_{W(waste)}$ and 50 μm pitch) is shown in Fig. 2, for several different heat transfer coefficients h on the rear of the 380 μm thick die. The ANSYS thermal simulation code (ANSYS Inc., Canonsburg, PA, USA) was used and further details of methodology and geometry are given elsewhere [6]. For each case, two temperature profiles are shown, one is the temperature on

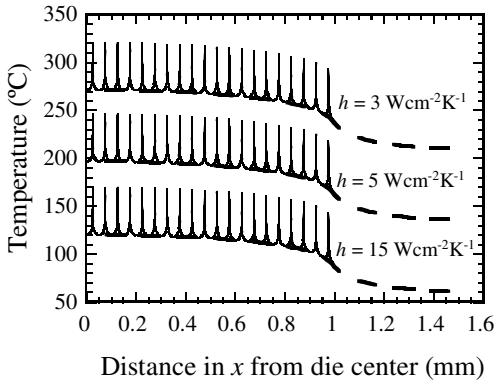

Fig. 2. Multi-finger MMIC temperature profile simulation, with thin lines representing a complete model and thick dashed lines based on the spatially-averaged assumption.

the top surface of the GaN layer taking into account the finger-based geometry of Fig. 1b, the other (thick dashed lines) is the profile using the spatially-averaged assumption. The underlying profile is well-modeled by the spatially averaged assumption, while the more detailed model including the localization of dissipation at the gates is required to predict the peak gate temperatures, which are about 50 °C hotter than the baseline profile in this example. High temperatures occur unless a very high heat transfer coefficient (above 15 W cm^{-2} K^{-1}) can be achieved. Microchannel coolers [7–9], which can achieve very high effective heat transfer coefficients, are a strong candidate for this application. The heat transfer properties, fundamental physics, and applications of microchannel coolers have been extensively described in the literature [10–13]. Microchannel coolers have been very successfully applied for high flux cooling of laser diodes [14–16] as well as in certain power switching and digital semiconductor devices [17–19]. However, very little published work exists on the use of microchannel coolers for dealing with the localized, extremely high heat fluxes that will occur in microwave amplifiers based on emerging GaN HEMT technology. Specifically, a simulation-based survey of thermal management options, including microchannel coolers, was performed by Kopp et al. [5]. Subsequently, the use of direct die-attached microchannel coolers for removing the heat from GaN-on-SiC MMICs with total dissipated powers above 100 W was explored theoretically with finite element simulations by Calame et al. [6]. However, experimental studies have been lacking.

The present article takes the research for this application to the next logical step, which is an experimental study of the removal of multi-kW/cm^2 heat fluxes from GaN-on-SiC semiconductor dies using microchannel coolers. The experiments involve a great variety of microchannel cooler materials and packaging geometries, which have not been previously applied to the task of cooling GaN-on-SiC devices. The article also investigates an emerging material, polycrystalline CVD SiC (with and without a diamond layer), for use in microchannel coolers, which has not been extensively documented in the literature. The experiments focus on removing the several kW/cm^2 heat fluxes levels expected to occur under the spatially-averaged assumption, over areas of 15 down to 6 mm^2. Detailed studies of temperature vs. power dissipation and flow rate are performed in microchannel coolers by themselves, and most importantly, in complete packages including dc-operated AlGaN/GaN-on-SiC heat source dies that are soldered directly to the microchannel coolers. The high thermal conductivity of the SiC semiconductor die material (Table 1) for emerging wide bandgap microwave amplifier applications, in comparison to the GaAs- and InP-based dies used in present microwave amplifiers [1] and laser diodes [14–16], allows for significant beneficial heat spreading and low temperature drops within the die itself. This leads to very effective overall heat transfer when combined with a microchannel cooler. The experimentally measured temperatures are also compared to ANSYS models that include both the die and the microchannel cooler. Overall, the article provides experimental demonstration of an effective thermal management strategy for the emerging, high-payoff transistor technology based on GaN-on-SiC HEMTs, which should enhance its transition to systems applications.

The article is organized as follows. In Section 2, details of the microchannel cooler geometries, fabrication techniques, and experimental setup are presented. In Section 3, a cartridge heater-based source is used to study the microchannel coolers in the absence of a semiconductor die. Then, in Section 4, the fabrication of the AlGaN/GaN-on-SiC heat source dies is described, and heat transfer measurements with these dies attached to AlN and Cu microchannel coolers are presented. The experiments with heat source dies are extended to Si and polycrystalline CVD SiC microchannel coolers in Section 5. In Section 6, the best performing microchannel coolers are tested with dies capable of creating 5 kW/cm^2 over 6 mm^2, to allow a direct comparison of behavior. These tests also include hybrid microchannel coolers employing a top layer of CVD diamond for added heat spreading. The article finishes with a discussion of theory vs. experiment in Section 7 and a summary in Section 8.

2. Fabrication and experimental setup

An assortment of fabrication methods were employed to create the microchannel coolers used in the experiments, depending on the material composition. For most non-metallic materials, such as polycrystalline AlN, thin rectangular pieces were obtained from a commercial supplier with the required overall dimensions of 12.70 mm long by 12.70 mm wide by 2.40 mm thick. The microchannels were cut in our laboratory by means of a diamond slitting saw blade. A diagram of this type of cooler is shown in Fig. 3a. There are seven channels, each 500 ± 25 μm wide by 1.4 ± 0.025 mm tall, with a center-to-center pitch spacing of 1.0 mm. The channel walls are vertical to within 2°. The surface roughness in a channel is typically ±3 μm, except

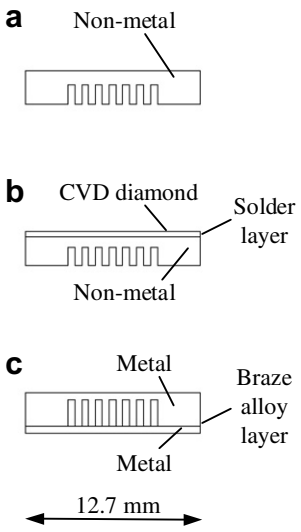

Fig. 3. Microchannel cooler cross sections.

at the entrance and exit corners where chip depressions as deep as 14 μm occur. A second configuration consisted of a non-metallic microchannel cooler capped with a layer of CVD diamond [16], as shown in Fig. 3b. The top of the microchannel cooler was metallized by electron-beam evaporation of 25 nm Ti, followed by 25 nm of Pt, and finally 400 nm of Au. CVD diamond, in the form of laser-cut 12.7 mm long by 12.7 mm wide by 400 μm thick slabs, was obtained from a manufacturer (SP3, Inc., Santa Clara, CA, USA) with a robust Ti/Au metallization already present. The diamond is of intermediate thermal quality, with a typical room temperature thermal conductivity of 1200 $W m^{-1} K^{-1}$ according to the manufacturer. The diamond was attached to the microchannel cooler in our facilities using Sn–3.5Ag solder (thermal conductivity of 33 $W m^{-1} K^{-1}$) and flux (#951, Kester Inc., Des Plains, IL, USA) at 240 °C, on a heated stage inside a glove box filled with nitrogen gas. The solder layer was typically 50 μm thick after joining.

A third type of microchannel cooler, shown in Fig. 3c, was made from oxygen free high conductivity (OFHC) copper. The two-part (closed channel) design was found to be necessary to prevent warping, due to differential thermal expansion and the softness of the copper, when the microchannel cooler gets joined with a semiconductor die later in the process [6]. The two-part microchannel cooler was made by machining a 12.7 mm long by 12.7 mm wide by 3 mm thick blank from bulk OFHC copper, followed by saw-cutting the seven channels. Tolerances and surface roughness are similar to those listed above. A bottom 1.5 mm thick OFHC copper plate was bonded to this piece using Cu–37.5Au high purity brazing alloy (Morgan Advanced Ceramics, Fairfield, NJ, USA) in an dry hydrogen furnace. Finally, the top and bottom surfaces were fly-cut on a milling machine to leave only 500 μm of copper above and below the channels.

The various heat sources that are used during the experiments, and the methods of attaching them or applying the heat externally, are described in Sections 3–6 below. Regardless of the type of heat source, the microchannel coolers during testing were mounted into a gasketted acrylic holder and manifold assembly, shown in Fig. 4. The brass top plate has a large hole to allow access to the top surface of the microchannel cooler for heat sources. The internal structure of the test cell is polished and designed to fit snugly around the microchannel cooler to a tolerance of 0.01 mm or better. The lower surface of the test cell interior acts as the bottom wall of the microchannels in the open channel designs of Fig. 3a and b.

The experimental setup for microchannel coolers uses water as a coolant and is based around a commercial chiller/gear pump/deionizer system with a constant 20 °C outlet temperature. The water flow is split into a secondary bypass loop and a main loop that passes through the microchannel cooler under test. Values on each loop allow accurate control of the water flow rate, and the flow through the microchannel cooler loop is measured with a turbine-based electronic flowmeter. Pressures are measured at the inlet and outlet ports of the test cell. Type J thermocouples are also located immediately adjacent to the test cell, with their sheathed junctions penetrating into the flowing fluid, to measure the differential temperature rise between the input and output of the test cell. The thermocouples are connected back-to-back and wired into a precision differential amplifier with the output displayed on a digital multimeter.

Extensive calibrations were performed to enhance the accuracy of the fluid calorimetry. The digital flowmeter was calibrated over the 0.72–3.8 l/min range by measuring, with a graduated cylinder, the volume of fluid (accuracy

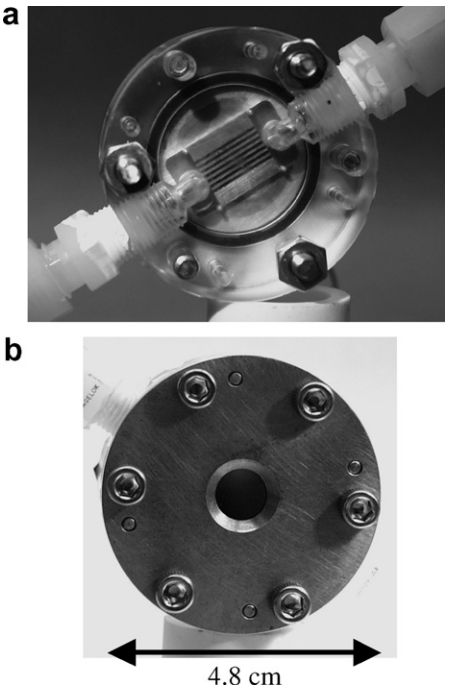

Fig. 4. (a) Bottom and (b) top views of the test cell containing a microchannel cooler.

±10 ml) passed in 60 ± 1 s. When combined with the additional ±0.016 l/min uncertainty due to the finite number of digits in the flowmeter, the overall accuracy of the calibration is ±3.5% at 0.76 l/min improving to ±1.8% at 3.8 l/min. The differential thermocouple setup was calibrated (with respect to thermocouple tables) using a 100 ± 0.5 °C temperature differential by immersion in boiling deionized water and an ice/deionized water mixture. Finally, the nominal differential amplifier gain of 99.7 was determined to within ±0.5% with a precision resistive divider. To test the overall calorimetry setup, a specialized heater (that allowed flowing fluid to directly contact a spiral nichrome wire) was mounted into the test cell. Power balance tests, involving a comparison between the electrical power supplied to the heater and the power measured via calorimetry, were performed. The calorimetric power was found by converting the measured differential voltage across the thermocouples into a differential temperature by means of thermocouple tables and the calibrations. This value, in conjunction with the known specific heat and flow rate of water, yielded the amount of power removed by the fluid. Measurements in the 20–120 W range at 0.72, 1.9, and 3.8 l/min flow rates indicated that respectively 94, 98, and 97% of the power applied to the heater could be found in the fluid.

3. Tests of microchannel coolers with an external cartridge heat source

The heat source used for initial testing was based on cartridge heaters. The idea was to create a hot spot on the top of a microchannel cooler that approximates the heat flux values/spot sizes that are expected to appear on the rear surface of semiconductor dies. Studying the behavior of the various microchannel coolers in isolation, without attached semiconductor dies, was felt to be a useful step towards understanding the behavior of complete packages. A partial schematic of the experimental setup is shown in Fig. 5. A set of four 300 W cartridge heaters were embedded lengthwise into a 3 cm diameter by 9 cm long copper rod. The output end of the rod was machined into a cone to taper down towards a flat 3.1 mm diameter tip, as can be seen in Fig. 5a. The main portion of the copper cylinder was insulated and suspended inside a water cooled housing (not shown), which allowed only the tip to protrude. A small flow of nitrogen and a coating of silver were used to limit oxidation.

A 3.1 mm diameter by 3 mm tall cylindrical metal adapter was mounted on the microchannel coolers, as seen in the lower portion of Fig. 5a and in Fig. 5b. For copper microchannel coolers, the adapter was simply soldered to the top of the microchannel cooler with Sn–3.5Ag solder. In the case of non-metallic microchannel coolers, thin Ti, Pt, and finally Au metal films were electron-beam evaporated onto the top surface, followed by attaching the adapter with Sn–3.5Ag solder. The microchannel cooler/adapter assembly was mounted in the gasketed test cell described in

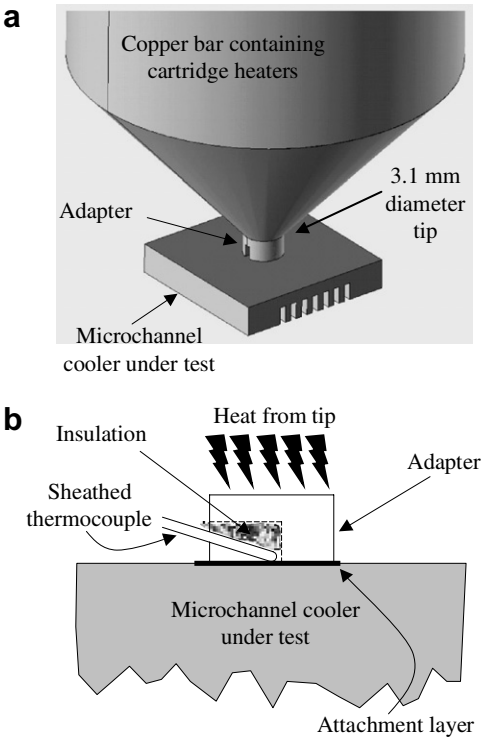

Fig. 5. Heat source for initial testing of microchannel coolers, showing (a) partial schematic and (b) cross section of adapter cylinder and thermocouple.

Section 2. The adapter had a 0.5 mm wide slot to allow placement of an ungrounded junction, type J thermocouple with a 0.25 mm OD stainless steel sheath on the top of the microchannel cooler, as can be seen in Fig. 5b (an insulating layer of fine Al_2O_3 fibers lies above and on the sides of the thermocouple). A drop of silver paint was applied to the tip of the thermocouple sheath prior to inserting it into the slot, to ensure thermal contact with the microchannel cooler.

To take experimental data, the tip of the heat source was aligned with an *x*-*y*-*z* stage and pressed downward onto the adapter cylinder. The temperature in the core of the heat source was stabilized with a feedback loop in conjunction with a separate sensing thermocouple, located in the center of the core. The power removed by the flowing fluid was measured by differential calorimetry, and the surface temperature on the top of the microchannel cooler was measured with the micro-thermocouple in the adapter cylinder. Steady-state temperatures in all quantities were typically achieved in about 2 min, provided modest increments in core temperature were used. Very high localized heat fluxes can be developed across the 3.1 mm diameter spot by virtue of the high core temperature (as high as 600 °C), the efficient heat removal by the microchannel cooler (resulting in a low surface temperature), and the conduction focusing action of the conical geometry.

The experimental results for OFHC copper and single crystal silicon microchannel coolers are shown in Fig. 6, for total flow rates of 0.72, 1.9, and 3.8 l/min. The differential

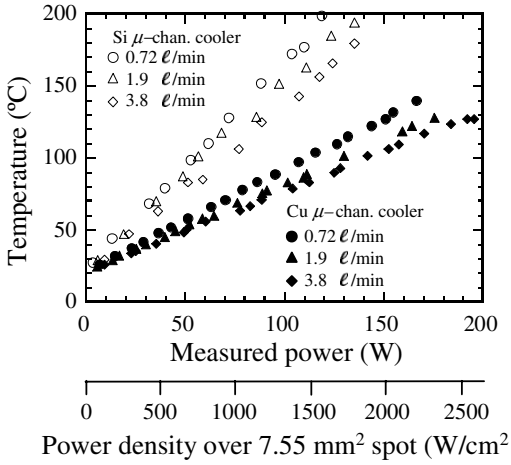

Fig. 6. Experimental data at various flow rates (l/min) for Cu and Si microchannel coolers obtained using the cartridge heater source.

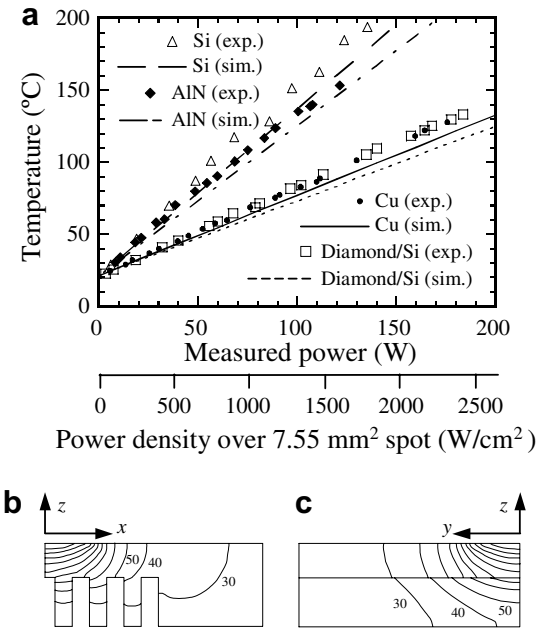

Fig. 7. (a) Experimental (exp.) data for various microchannel coolers at 1.9 l/min flow rate, obtained using the cartridge heater source, along with ANSYS simulations (sim.) shown by lines; (b), and (c) simulated temperature contours in the central xz and yz section views, respectively, inside the AlN microchannel cooler with 1600 W/cm^2 applied to the heated spot (30–130 °C by 10 °C contours shown).

pressures required to achieve these flow rates in the silicon microchannel cooler, including the manifold assembly, were 0.05, 0.21, and 0.83 bar, respectively. The corresponding linear flow velocities within the channels were 2.6, 6.5, and 13 m/s respectively. In the plots of Fig. 6, the "measured power" that is being plotted on the horizontal axis is obtained directly from the fluid calorimetry. This power, combined with the known 3.1 mm diameter of the heat source tip, is used to obtain the localized heat flux, which is provided as a second x-axis in the plot. The vertical axis in the plots is the measured surface temperature of the microchannel cooler, obtained with the micro-thermocouple. The lower surface temperatures obtained with the copper microchannel cooler compared to silicon are due to the much higher thermal conductivity of copper, as expected intuitively. The effect of flow rate is modest; for example, doubling the flow rate from 1.9 to 3.8 l/min in the copper case only reduces the temperature from 118 to 108 °C at 160 W of power.

Fig. 7a is a plot of the measured behavior (symbols) of a wider variety of microchannel coolers at 1.9 l/min. The Si and Cu data are from the previous figure. New results are plotted for a polycrystalline hot pressed AlN microchannel cooler and a hybrid CVD diamond-on-single crystal Si microchannel cooler. The AlN cooler had the geometry of Fig. 3a, while the diamond-on-silicon cooler had the geometry of Fig. 3b. As can be seen in Fig. 7, the AlN microchannel cooler has a behavior slightly better than Si. Furthermore, while adding the diamond layer on top of a silicon microchannel cooler greatly improved the performance (compared to silicon by itself), the heat transfer characteristics of the diamond/silicon hybrid are essentially the same as those of the copper microchannel cooler.

The experimental results at 1.9 l/min were compared to finite element simulations with the ANSYS thermo-mechanical code. In this initial round of simulations, temperature-independent thermal conductivities were used (Si, AlN, Cu, and diamond $\kappa = 150$, 180, 385, and 1200 W m^{-1} K^{-1}, respectively). A three-dimensional ANSYS model based on free-meshed tetrahedral finite elements (10-nodes/element, ~2300 elements) was created for the appropriate microchannel cooler geometry (from Fig. 3) and material composition, with a 3.1 mm diameter circular spot on the top receiving a specified heat flux F_H. A relatively fine meshing was used under the heated spot (~0.22 mm tetrahedron edge length), which gradually transitions (element edge expansion factor of ~1.2) to a coarser mesh towards the microchannels and the more remote regions of the model. Great care was required to mesh the diamond-on-silicon hybrid microchannel cooler, as the joining solder layer is thin. In this case, 10-node tetrahedra with a ~50 μm vertical and ~0.16 mm transverse edge lengths were used in the solder layer, and tetrahedra with ~0.10 mm edge lengths were used for the diamond layer in the vicinity of the heated spot. Gradual transitions were again used between these densely-meshed regions and a coarser mesh used in the more remote regions of the model space, and the resulting model had ~39,600 total elements.

For all the models, the remainder of the top surface (outside the heated spot) was treated as thermally insulating, as were all of the side surfaces. The channel walls were assigned an appropriate convection coefficient h_{wall} as a boundary condition in ANSYS. Specifically, at 1.9 l/min, the 6.5 m/s linear flow velocity in the channels of Fig. 3a corresponds to a Reynolds number Re of 4740, which is turbulent. This assumes each channel has a hydraulic diameter D equal to four times the channel area divided by the channel perimeter, which works out to $D = 2td/(t + d) = 0.74$ mm for the $d = 500$ μm by $t = 1.4$ mm channel dimensions. Using a friction factor f approximated by

$$f = (1.58 \ln Re - 3.28)^{-2} \quad (1)$$

and the Petukov–Kirrillov correlation [20] for Nusselt number Nu

$$Nu = \frac{(f/2)\,Re\,Pr}{1.07 + 12.7\sqrt{f/2}(Pr^{2/3} - 1)}, \quad (2)$$

one obtains a channel wall convection coefficient $h_{wall} = Nu\,\kappa_f/D$ of 3.85 W cm^{-2} K^{-1}, where κ_f is the thermal conductivity of the water. A fluid bulk temperature T_B of 20 °C was assumed.

The results of the simulations for the different microchannel cooler materials are shown by the various lines in Fig. 7a. Overall, the agreement between the simulations and the experiments is rather good, with the measured temperatures being about 10% higher than the simulations. Convergence of the modeling with respect to element size was investigated by reducing the element edge sizes by a factor of two in the region beneath and nearby to the heated spot, including the microchannel fins (e.g., increasing the number of elements in the AlN case from ~2300 to ~7300). The changes cause only a ~0.15% increase in the predicted temperature rise (relative to T_B), which indicates that the coarser mesh was sufficient and that convergence has been obtained. We also note that the rise in bulk fluid temperature due to heat absorption from the channel walls or from viscous heating [21,22] are both relatively minor effects under the experimental conditions. Specifically, the bulk rise due to heat absorption at a total flow of 1.9 l/min, averaged across the seven channels, is only 1.2 °C at 160 W of absorbed power. Furthermore, the assumption of constant viscosity is reasonable, since the bulk rise would only result in a decrease in viscosity from 1002 to 977 μPa s. The impact of viscous heating, which can be an issue at high Re in microchannels, can be estimated by examining the dissipated pumping power (delta pressure × volume flow) and computing the corresponding additional bulk temperature rise [21]. At 1.9 l/min flow and with the measured differential pressure of 0.21 bar, the pumping power is 0.67 W, which when dissipated in the fluid, would cause only a negligible ~0.005 °C addition to the bulk temperature.

One can conclude from this section that the localized heat flux capabilities of the microchannel coolers are consistent with the requirements for cooling the rear surfaces of the dies of GaN-on-SiC devices. Effective heat transfer coefficients between the small heated spot and the fluid, given by the average slopes of the experimental temperature data in Fig. 7a with respect to the power density axis, are found to be 10 and 12 W cm^{-2} K^{-1} for the Si and AlN cases, respectively, and about 21 W cm^{-2} K^{-1} for both the copper and hybrid diamond/silicon cases. The localized high heat flux capability is due primarily to the small size of the heated region and dilution of heat flux by three-dimensional spreading as it flows into the body and fins of the microchannel cooler, in addition to the substantial values of h_{wall} achievable in the channels. The critical role of heat spreading can be visualized by the temperature contours in Fig. 7b and c, which are obtained from an example ANSYS simulation of the AlN microchannel cooler with $F_H = 1600$ W/cm^2 applied to the heated spot. Only one-half of the cross section views in the central xz and yz planes are shown. In the solid region below the heated spot (and above the channels), the heat flowing away from the spot is approximately hemispherical, which quickly brings the flux to manageable levels with modest temperature drops. For example, the peak temperature in the center of the spot is 144 °C, but halfway down towards the channel top, the heat flux has fallen to 1000 W/cm^2 at a temperature of 106 °C. By the time the central channel top wall is reached, the flux is only 250 W/cm^2 and the temperature is 86 °C. Such flux levels are easily handled by the aggressive convection in the channels. Additional heat spreading occurs as one proceeds downward through the fins. Detailed studies of the combined three-dimensional thermal conduction and convective behavior of microchannel coolers are available in the literature [23,24].

4. Tests of AlN and Cu microchannel coolers with GaN-on-SiC heat source dies

Having tested the microchannel coolers under high heat flux using the cartridge heater assembly, the next logical step was to create and test more realistic packages that used actual GaN-on-SiC semiconductor dies attached to microchannel coolers. This was intended to include the impact of thermal conduction through the die itself and the die-attach solder layer on peak temperatures in the

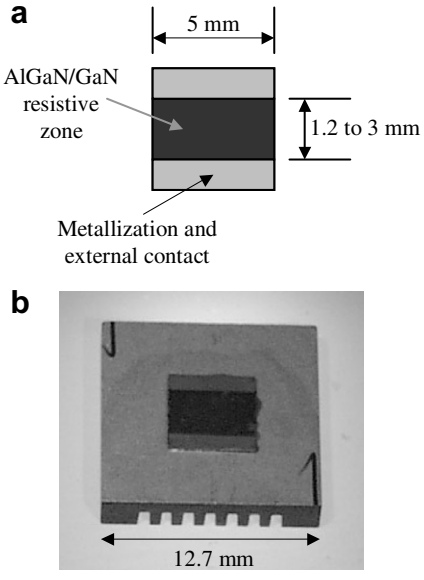

Fig. 8. (a) Diagram of GaN-on-SiC heat source dies and (b) photograph of a die with a 3 × 5 mm^2 resistive zone attached to an AlN microchannel cooler.

semiconductor, in a geometry of relevance to the active region of a MMIC (under the spatially-averaged assumption). A diagram of such a die is shown in Fig. 8a. They were fabricated by a multi-step process that began with the purchase of a 5.1 cm diameter, 380 μm thick 4 H–SiC semi-insulating SiC wafer (Cree, Inc., Durham, NC, USA). A 100 nm thick AlN nucleation layer, followed by a 1 μm thick layer of undoped GaN, were deposited on the top of the wafer using molecular beam epitaxy (MBE) techniques in our laboratory. This was followed by growing about a 30 nm of AlGaN. Such a vertical heterostructure creates an electrically conductive sheet of charge near the junction between the AlGaN and the undoped GaN. Ohmic contacts were placed and annealed to make electrical connections to the charge layer and to define the boundaries of the electrically resistive zone between the contacts. Gold metallization pads were placed over the ohmic contacts. The rear surface of the wafer was metallized using the Ti/Pt/Au thin film scheme described earlier, to allow die attach with solders. Finally, the wafer was cut into $5 \times 5\ \text{mm}^2$ individual dies with a diamond-bladed dicing saw.

One of the $5 \times 5\ \text{mm}^2$ dies with a 3 mm long by 5 mm wide resistive zone was die-attached to a top-surface-metallized AlN microchannel cooler (of the style in Fig. 3a) using Sn–3.5Ag solder and Kester 951 flux at 240 °C, in N_2 gas. The die-attach layer thickness was 50 ± 5 μm. A photograph of the resulting package is shown in Fig. 8b. The package was placed in the test cell, and electrical leads were mounted to the gold contacts using silver paint. A 0.50 mm diameter, ungrounded sheath, type J thermocouple was placed on the center of the resistive zone of the die using a drop of silver paint (smaller than the sheath diameter). As the resistive zone is only insulated by the ~30 nm of AlGaN, and quite high voltages (600 V) are used to energize the die, the entire thermocouple and battery-powered thermocouple meter assembly are floating relative to ground and are enclosed in an insulating plastic box for safety. To make thermal measurements, a desired energizing voltage was applied to the resistive zone of the die, and the surface temperature and differential flowing-fluid temperature rise were monitored until steady-state was reached in both quantities. The energizing voltage and current were also noted, to allow independent confirmation of the power being dissipated in the resistive zone of the die. Between measurements the power was removed, and the temperature was allowed to cool back to the bulk fluid temperature. The process was repeated using higher and higher energizing voltages, to create a complete dataset.

The experimental results at 1.9 l/min flow rate, for the package using the AlN microchannel cooler, are shown by the circle symbols in Fig. 9. The horizontal axis shows the power removed via fluid calorimetry, while the second horizontal axis shows the derived power density on the top of the die. The power density was obtained by dividing the power based on fluid calorimetry by the size of the resistive zone ($0.15\ \text{cm}^2$). A concave-upwards curvature is visible in the data, which is consistent with temperature-dependent thermal conductivity effects in the silicon carbide, and to a lesser extent, the AlN. To investigate this further, an ANSYS simulation was performed, using temperature-dependent thermal conductivities for 4 H–SiC and polycrystalline AlN [25]. Tetrahedral (10-node) meshing elements were employed in the die with mesh edge lengths of ~0.25 mm under and near the resistive zone, while the thin die attach was modeled with tetrahedra of 50 μm height and ~120 μm transverse size. Gradual transitions were used between these regions and the courser-meshed microchannel cooler, resulting in a model with ~12,100 total elements. The temperature-dependent thermal conductivity curves used in the simulations are shown in Fig. 10, along with curves for other materials [26] to be discussed later. The thermal conductivity of the die-attach solder was held fixed at the room temperature value. Each simulation (for a given power dissipation) was run using the ANSYS nonlinear iterative process, with a requirement of at least five equilibrium iterations and that the difference between the applied heat flow and the computed internal heat flow is less than 0.5% at the termination of the iterations. Nonlinear convergence was further checked forcing

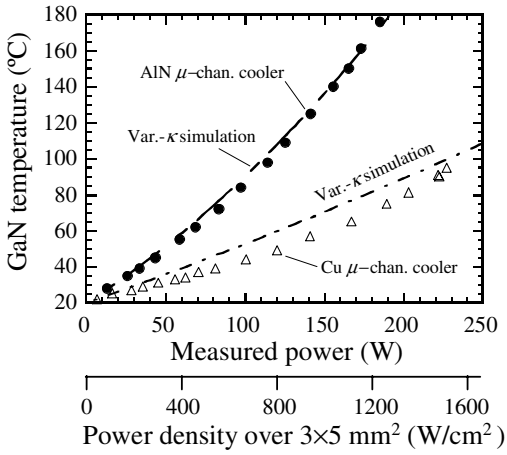

Fig. 9. Experimental results and ANSYS simulations of AlN and Cu microchannel coolers at 1.9 l/min, using GaN-on-SiC dies with a $3 \times 5\ \text{mm}^2$ resistive zone as a heat source.

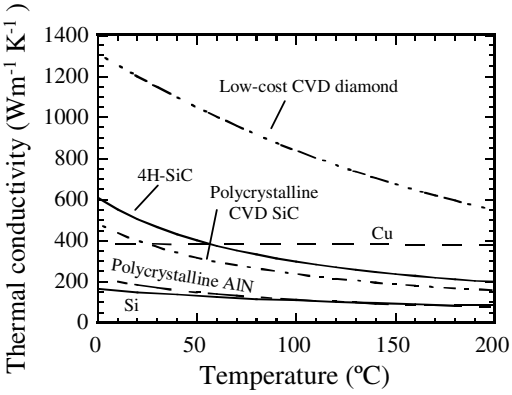

Fig. 10. Temperature-dependent thermal conductivities of materials.

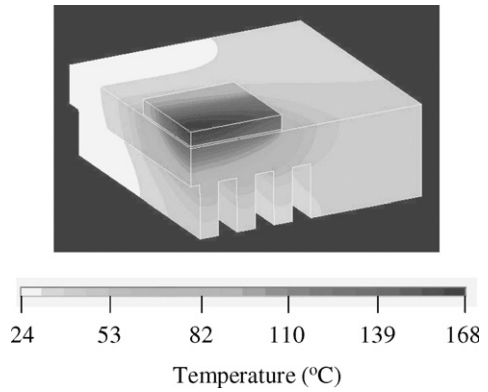

Fig. 11. ANSYS simulation for the AlN microchannel cooler and heat source die at 180 W power.

an additional two iterations and ensuring that simulated temperatures did not change more than 0.5%. The simulation results are shown by the long-chain-link line in Fig. 9, and the agreement is excellent. A contour plot of the temperature distribution from the ANSYS simulation is shown in Fig. 11 at the highest power (180 W), with only one-fourth of the model space shown (the center of the resistive zone is at the front-left-top corner of the model).

Experiments were also conducted with a die that was attached to an OFHC copper microchannel cooler with Sn–3.5Ag solder, with the geometry of the cooler shown in Fig. 3c. The die size and resistive zone size were maintained at $5 \times 5\ mm^2$ and $3 \times 5\ mm^2$, respectively. The measured die-attach layer thickness was only about 6 μm in this package, which was probably caused by a larger vertical force being applied during the die-attach process. Experimental measurements of peak die temperature vs. power are shown by the triangle symbols in Fig. 9. An ANSYS simulation, using temperature-dependent thermal conductivities for the SiC and the copper, is shown with the short-chain-linked line. Meshing with 3 μm thick and ~80 μm wide, 20-node brick elements was used to resolve the die-attach layer in the simulation, while the resistive zone of the die was meshed with tetrahedra with ~65 μm edge length. Once again, gradual transitions with tetrahedral and pyramidal elements were used between these regions and into the coarser-meshed microchannel cooler (model has ~50,500 elements). The agreement between the simulation and experiment is not as good as in the AlN case, with the experimental temperature values in the Cu case being lower than the simulation. We note that 98% of the dissipated electrical power is found in the fluid (via calorimetry), ruling out parasitic heat losses as a cause of discrepancies between theory and experiment.

5. Tests of Si and polycrystalline CVD SiC microchannel coolers

In order to explore somewhat higher power densities and further expand the various combinations of dies and microchannel cooler materials being studied, additional experiments were performed using dies with a 2 mm long by 5 mm wide resistive zone. The overall die size was maintained at $5 \times 5\ mm^2$. A set of experiments was performed with one of these dies attached to a single crystal silicon microchannel cooler. The top of the cooler was metallized as before, but the die attach was made with Sn–3.5Ag–0.5Cu. This die-attach material ($\kappa = 55\ W\ m^{-1}\ K^{-1}$) is under heavy investigation worldwide for use as a lead-free replacement for Sn–Pb solders. The attachment was done in N_2 gas at 245 °C using Kester 951 flux followed by washing in isopropanol. Subsequent measurements indicated a die-attach thickness of about 6 μm.

Experimental data obtained at three different flow rates with the silicon microchannel cooler is shown by the solid symbols in Fig. 12. A considerable reduction in temperature at a given power level occurs when the flow is increased from 0.72 to 1.9 l/min, but the reduction is much more modest with a further increase of the flow to 3.8 l/min. The relatively low thermal conductivity of silicon limits the benefits afforded by a large convection coefficient in the channels. The results of a 34,000 element ANSYS simulation for the heat source die on the silicon microchannel cooler at 1.9 l/min is shown by the solid line in Fig. 12. The simulation, which assumed temperature-dependent thermal conductivities in all non-metallic materials, indicates moderately higher temperatures compared with the experimental data.

Experiments were also performed using a polycrystalline CVD SiC microchannel cooler. This material was added to the roster of experiments for a number of critical reasons. First, the material presents the opportunity for a nearly perfect thermal expansion match to the 4H–SiC dies that are used in GaN-on-SiC devices. Second, in spite of the polycrystalline nature of the material, the room temperature thermal conductivity can be an extremely high 380–400 $W\ m^{-1}\ K^{-1}$, rivaling that of copper. This is due to the material being directly made into bulk polycrystalline

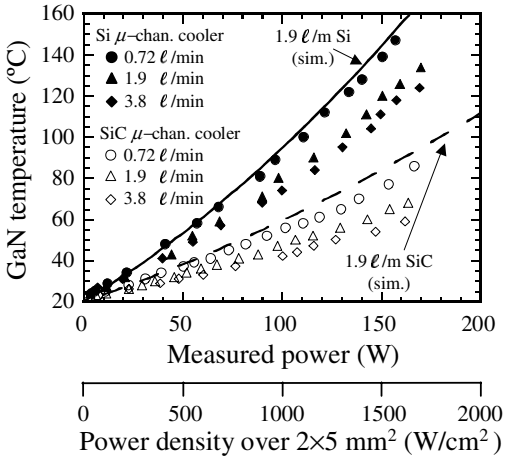

Fig. 12. Experimental results (symbols) for Si and polycrystalline CVD SiC microchannel coolers at various flow rates, using GaN-on-SiC dies with a $2 \times 5\ mm^2$ resistive zone as a heat source. Corresponding ANSYS simulations (sim.) at 1.9 l/min are shown by the lines.

monoliths by chemical vapor deposition, as opposed to hot pressing or sintering SiC particulate powders. Finally, the material is over a factor of 10 cheaper than single crystal 4H–SiC or 6H–SiC, and it can be obtained in relatively large shapes.

Polycrystalline CVD SiC was obtained commercially (Rhom and Haas, Woburn, MA, USA) and diamond-machined into a microchannel cooler of the same dimensions as used in the AlN and Si experiments. Metallization, and attachment of a $5 \times 5\ mm^2$ GaN-on-SiC die with a $2 \times 5\ mm^2$ resistive zone using Sn–3.5Ag–0.5Cu, were performed. Experimental measurements of the GaN temperature as a function of dissipated power are shown by the open symbols in Fig. 12. The package runs much colder than the Si-based package, by about a factor of two in temperature rise at a given power. The data, combined with the advantages in expansion coefficient matching, indicate that polycrystalline CVD SiC is a promising material for this application. An ANSYS thermal simulation (~34,000 elements) was performed for the 1.9 l/min situation. The thermal conductivity of polycrystalline CVD SiC was approximated by taking the functional form of the 4H–SiC thermal conductivity vs. temperature curve, and rescaling it so that the 20 °C value was $400\ W\ m^{-1}\ K^{-1}$. The ANSYS results are shown by the dashed line in Fig. 12. The experimental temperatures lie below the simulation.

6. Extremely high heat flux comparative tests

The most promising material systems and configurations from the experiments of Sections 3–5 were selected for a final set of experiments that allow direct comparison of package performance at even higher heat flux levels. The microchannel coolers selected were the two-part copper cooler, the polycrystalline CVD SiC cooler, and the CVD diamond-on-silicon cooler. A fourth case, CVD diamond-on-polycrystalline CVD SiC, was added to the list. This was based on the excellent behavior of the SiC material by itself and the belief that even better performance would be achieved in conjunction with diamond. To reach extremely high heat fluxes, a new set of GaN-on-SiC dies having smaller resistive zones (5 mm wide by 1.2 mm long) was fabricated. The physical die size remained at $5 \times 5\ mm^2$ by 380 μm thick. The dies were attached to the metallized microchannel coolers using ~6 μm of Sn–3.5Ag–0.5Cu solder.

Experimental results for the four packages are shown in Fig. 13. One can see from the figure that the behaviors of the copper, the polycrystalline CVD SiC, and the CVD diamond-on-silicon coolers are very nearly the same. The agreement between the copper and the CVD diamond-on-silicon microchannel coolers is not surprising, given the similar results obtained during the cartridge heater tests. The additional fact that the polycrystalline CVD SiC microchannel cooler has temperatures comparable to copper (or even slightly lower) is extremely encouraging, and it reinforces the belief that this material has a thermal

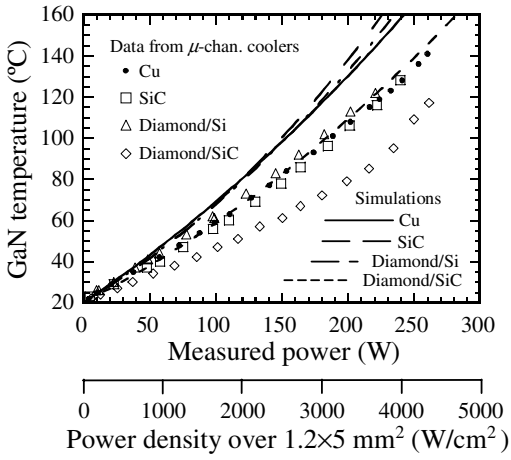

Fig. 13. Experimental results (symbols) for various microchannel coolers at 1.9 l/min using GaN-on-SiC dies with a $1.2 \times 5\ mm^2$ resistive zone as a heat source, with ANSYS simulations shown by lines.

conductivity at least as high as copper. When one considers that the expansion-matched SiC microchannel cooler should produce relatively little stress on the SiC die (vs. a high stress using copper [6]), the comparable temperature levels obtained with the SiC material are even more noteworthy.

The temperature levels of the CVD diamond-on-polycrystalline SiC hybrid are significantly lower in comparison to the other packages. At intermediate power levels, the temperature rise (relative to 20 °C) is about 30% less than for the SiC alone, but this advantage decreases to about 20% at the highest power level studied. This is due to the rapid fall-off in diamond thermal conductivity with temperature. A detailed experimental comparison between the polycrystalline CVD SiC microchannel coolers with and without the diamond layer is shown in Fig. 14. Very high power levels (250–300 W) and heat fluxes (4–5 kW/cm² over

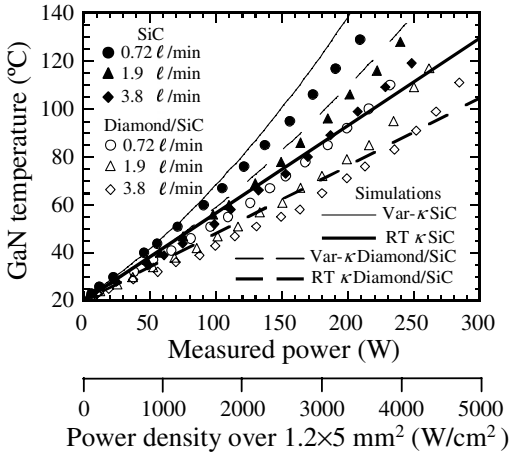

Fig. 14. Experimental data (symbols) for polycrystalline CVD SiC microchannel coolers at various flow rates with and without diamond, using GaN-on-SiC dies with a $1.2 \times 5\ mm^2$ resistive zone as a heat source. The lines show ANSYS simulations at 1.9 l/min using temperature-dependent (var-κ) and constant room temperature (RT κ) thermal conductivities.

the small $1.2 \times 5\ mm^2$ resistive zone) can be effectively managed while maintaining temperatures below 120 °C in the GaN. It is noteworthy that the diamond-on-polycrystalline CVD SiC package at 0.72 l/min has temperatures comparable to the package without the diamond at the much higher 3.8 l/min flow rate. Thus, the diamond-containing package can be used to greatly reduce the required flow rate of water, which is an important issue in systems applications. There is also little evidence of saturation in power handling capability as a function of flow rate, which is quite different from some of the earlier packages based around lower thermal conductivity materials. Thus, in situations where additional flow can be provided, significantly higher powers should be manageable. However, as with the diamond-on-Si package [6], the diamond-on-polycrystalline SiC microchannel cooler will place the die under considerable tension which can have negative impacts, particularly on reliability. Further study is needed to explore these various tradeoffs from an applications standpoint.

7. Discussion on simulations vs. experiments

Regarding comparison between simulation and experiment, a number of observations can be made. In Fig. 13, ANSYS simulations (including temperature-dependent thermal conductivities) for the 1.9 l/min flow rate are shown by the lines. The number of elements in the simulations was ~26,200 (for the cases involving diamond, ~48,400). The experimental temperatures at high powers lie significantly below the simulations in all cases. This follows a general pattern of discrepancy that was observed to a lesser extent in the dies with a $2 \times 5\ mm^2$ resistive zone. In spite of this, the Fig. 13 simulations for the dies with $1.2 \times 5\ mm^2$ resistive zones do show nearly identical relative performance between the copper, polycrystalline SiC, and diamond-on-silicon microchannel coolers, in agreement with the experimental trends. Similarly, the relative lower temperatures in the diamond-on-polycrystalline CVD SiC microchannel cooler simulation, in comparison to the other simulations, is also evident.

There are a number of possible explanations for the deviations between experiment and simulations. One possibility that immediately comes to mind is the choice of convection coefficient inside the channels; if the actual convection were higher than Petukov–Kirillov theory, then the simulated temperatures would be lower. After all, features like surface roughness and imprecision in the geometry at the channel entrances were not included in the analysis, and such factors influence the effective hydraulic diameter, Reynolds number, and particularly the friction factor [27,28]. For example, at 1.9 l/min flow, a recalculation of the friction factor with the ±3 μm surface roughness [29] increases f from 0.0098 to 0.012, which results in a 10% increase in Nu and h_{wall}. However, this only causes a small reduction in the computed temperatures in Fig. 13; for example, in the Cu case at 200 W, the temperature is reduced by only 1.4 °C. Furthermore, gross inaccuracies in the convection coefficient are difficult to justify given the results from the cartridge heater studies in Section 3, in which the data for the microchannel coolers by themselves (i.e., without dies) were in good agreement with simulations.

A more likely explanation for the discrepancy is suggested by closely examining Fig. 14, in which the simulations at 1.9 l/min using temperature-dependent thermal conductivities are shown using the thin lines. The slopes of these simulation curves are actually in quite good agreement with the slope of the data at low powers. This indicates that the room temperature thermal conductivity values are likely accurate. Simulations with the thermal conductivities held constant (at 20 °C values) are shown by the thick lines in Fig. 14. The 1.9 l/min experimental data stays reasonably close to these lines initially, then gradually rises above the lines at higher powers due to temperature-induced reductions in thermal conductivity. The departure never reaches the severe extent predicted by the temperature-dependent simulations, however. This implies that the decrease in thermal conductivity with temperature is less than assumed. The discrepancies in Figs. 12, 13, and 9 (for Cu) show a similar pattern.

As far as which material is exhibiting less roll-off in thermal conductivity than expected, the most likely candidate is the 4H–SiC die [25]. The most convincing justification for this can be found from the data for the silicon microchannel cooler in Fig. 12; since silicon is such a well-known material, it is highly unlikely that the published thermal conductivity values for silicon are the cause of the deviation. The only fact that contradicts this picture is the excellent agreement obtained with the AlN microchannel cooler in Fig. 9 using the published values for 4H–SiC. However, this particular package had a thick (~50 μm) die attach of poorly conductive solder, compared to the ~6 μm thick die-attach layers used in all the other experiments. The thick solder layer in the AlN package contributes ~30 °C to the total temperature rise at the highest power studied. This thermal resistance tends to linearize the overall thermal response, and places the die into a much more isothermal state, which arguably renders the calculation less sensitive to variations in the 4H–SiC properties. Clearly, further work is needed on measuring the temperature-dependent thermal conductivities of the 4H–SiC and the other less well-studied materials actually used in the various packages, including polycrystalline CVD SiC and the low-cost CVD diamond.

8. Summary and future prospects

Experiments on removing high heat fluxes from GaN-on-SiC semiconductor dies using microchannel coolers have been performed. The dies contained an AlGaN/GaN heterostructure that was operated as a direct current resistor, providing a localized heat source. The dimensions of the heat source were sized to represent the spatially-averaged heat flux that would appear in MMICs. A wide

variety of materials and configurations were investigated, allowing a comparison of the microchannel cooler performance and the resulting GaN temperatures. Silicon and AlN microchannel coolers exhibited good performance at lower power densities (1000–1200 W/cm^2 over 3×5 mm^2 to 2×5 mm^2 resistive zones). Polycrystalline CVD SiC microchannel coolers were found to be extremely promising for higher power densities (3000–4000 W/cm^2 over 1.2×5 mm^2 resistive zones with 120 °C GaN temperature). The performance was as good as a copper microchannel cooler, but presumably without the stress problems associated with differential thermal expansion between the semiconductor die and copper. No advantage was found for a hybrid microchannel cooler consisting of low-cost CVD diamond-on-silicon; it performed similarly to polycrystalline CVD SiC yet the package is much more complex. However, a hybrid microchannel cooler consisting of low-cost CVD diamond on polycrystalline CVD SiC exhibited moderately better performance (20–30%) than polycrystalline CVD SiC alone. While diamond has been shown to allow either a higher heat flux or a lower water consumption, the package complexity and issues of differential expansion stress may prove problematic. All packages described in this article, regardless of their material composition, need further investigation for reliability under thermal cycling.

Good agreement between theory and experiment was found for the thermal behavior of microchannel coolers tested using the cartridge heater source. For the more complex packages that included GaN-on-SiC semiconductor dies as heat sources, in general the experimental GaN temperatures were somewhat lower than the temperatures predicted by ANSYS simulations. The effect appears to be related to the temperature-dependent thermal conductivity effects in the specific materials employed in the packages being different from the behavior suggested from published literature. The 4H–SiC die material was thought to be the most likely culprit. Additional experiments to measure temperature-dependent thermal conductivity in materials of interest for microchannel coolers and semiconductor dies are suggested.

Finally, since the resistive zone layout on the dies was based on a spatially-averaged approximation, the localized gate temperatures in an multi-fingered MMIC would be higher than measured in these experiments. Prior simulations indicate local additional heat rises of 50–60 °C right under the gates [4–6] at 5 W/mm dissipation per unit gate width. Thus, using the typical value of 120 °C observed in the present experiments with the spatially-averaged heat source dies, one would expect peak gate temperatures of 170–180 °C in a GaN-on-SiC MMIC. Temperatures at that level would be nominally acceptable for many applications. Additional experimental work is therefore needed on microchannel coolers attached to dies with a completely realistic multi-finger source–gate–drain geometry, to measure the localized gate temperatures and compare to simulations. It would also be useful to use an infrared camera to obtain the overall spatial temperature distribution across the dies.

Acknowledgements

This work was supported by the Office of Naval Research. The authors thank D.S. Katzer for MBE growth, N. Green for GaN device fabrication, and A.N. Smith for useful discussions.

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